Statistical Computer-Aided Design for Microwave Circuits

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Abstract—**A useful methodology for microwave circuit design is presented. A statistical technique known as Design of Experiments is used in conjunction with computer-aided design (CAD) tools to obtain simple mathematical expressions for circuit responses. The response models can then be used to quantify response trade-offs, optimize designs, and minimize circuit variations. The use of this methodology puts the designer's intelligence back into design optimization while making "designing for circuit manufacturability" a more systematic and straightforward process. The method improves the design process, circuit performance, and manufacturability. Two design examples are presented in context to the new design methodology.**

I. Introduction

IT IS DIFFICULT to meet the rigorous performance requirements that are needed in today's competitive microwave circuit market. The design process eventually becomes a series of choices made by evaluating circuit performance trade-offs. Unfortunately, the process of making these choices is more of an art than a science due to the complex relationships driving a circuit's responses. The response relationships make design trade-offs difficult to quantify and therefore are seldom used to the designer's advantage. Performance optimizers compound the problem by being extremely sensitive to the user-weighted performance objectives. Computer optimization routines can create impossible circuit parameter combinations, design circuit responses that are too sensitive to parameter variations [1], or end up getting trapped in a local minimum without reaching the optimization goals. However, a statistical technique known as Design of Experiments (DoE) can be used in addition to the current design process in order to make circuit design easier and more systematic.

Design of Experiments is a well established area of statistics that is used to make deliberate changes to the input variables of a system in order to identify differences in the system's output responses. Response changes can be fitted using standard statistical regression techniques to simple mathematical functions of the system's input variables. The expressions are approximations in a particular region of the circuit's designable parameter values and reveal important response trends. The coefficient estimation of a regression model fits a linear equation for a product's response as a function of the input variables representing a circuit's designable parameters. Interactions between parameters and nonlinear terms can also included in the response model. The types of circuit responses that can be characterized can be anything such as simple amplifier gain, amplifier noise figure, or circuit input impedance. The power of this methodology is obtaining simple empirical expressions for the product's response which can be used by a designer to gain insight to the trends within some region of parameter space.

Taguchi introduced the DoE techniques to engineering for quality improvement [2]. In the past, enhancements to the DoE technique have been used on a production line or laboratory to derive empirical models and optimize a given process. This approach is called response surface methodology (RSM) and is becoming increasingly popular in American industry. However, the DoE technique may be incorporated within computer-aided design (CAD) packages to give engineers a powerful, yet simple, design tool [3]. A computer can perform "virtual" experiments using the DoE's systematic methodology and produce a simple expression which will almost always be less complex than the true physical relationships that govern circuits. The empirical expression can then be used to better understand the effect of design variables, either alone or in combination, on a circuit's response. This approach to empirical modeling will be called statistical computer-aided design (SCAD) in this paper. SCAD is useful in the design environment because it can be used to quantify performance trade-offs, perform goal optimization, and minimize circuit variability. This combination of statistical techniques and CAD can enable bad circuit designs to become good and good designs to become even better.

This paper presents the use of the SCAD methodology for microwave circuit design. The basic DoE concepts and terms are presented to give an overview of the methodology and to supplement other papers on the subject [4], [5]. The intent of this research is to introduce the microwave circuit designer to a new and beneficial way to design circuits for not only nominal performance but for manufacturability. It should be emphasized that this statistical design methodology is a useful alternative, not a replacement, to the current design tools already available to the engineer. The SCAD methodology will be demonstrated in this chapter on two microwave amplifier design examples.

II. DoE Background

Many of the DoE concepts were popularized by Taguchi's contributions to the methodology of off-line quality design. The basis for his approach is to minimizing the "loss to society" that occurs when a product's performance varies from a customer-specified target [6]. Taguchi's ideas for param-

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eter and tolerance design have evolved into what industry labels Design of Experiments for robust product design. The DoE technique describe parameter settings that maximize the amount of extractable information in the minimum number of experimental runs, or computer simulations, for fitting a regression model to a system response. This aspect is a benefit to both physical and virtual experiments because it uses the minimum amount of resources (time, money, or computer) to achieve accurate modeling.

What makes the DoE approach so powerful is that all of the significant controlling parameters are changed simultaneously according to predetermined levels. This is much more effective than other nonstatistical methods used by engineers and scientists [3] because important factor interactions can be missed when just changing one variable at a time. In the DoE methodology, all of the variables that can affect a product's performance, such as lengths, doping densities, temperatures, or capacitance, are called factors. The values that the factors are assigned are *levels*. There are *designable factors* which an engineer can control to make the product perform in a desirable way. Examples of these are a circuit's capacitance, transmission line length, and doping levels. *Noise factors*, or sometimes called *environmental factors*, are those which the designer can not control such as aging effects, temperature, or natural processing variations in the designable component values. One can only minimize the effect of the environmental factors on circuit response by favorable design choices. It should be mentioned that in the DoE approach both types of factors must be independent, or orthogonal, to each other such that changing one variables value does not affect any of the others when using the DoE techniques. An *experiment* is when all of the factors are assigned a particular value or level. In a DoE, each variable would be assigned its value for the experiment, and the outputs or responses would be recorded for statistical analysis and model fitting. Examples of the most useful experimental designs for SCAD modeling are full and fractional factorial, central composite, and box-Behnken [7].

Full factorial experimental designs are those in which all possible combinations of factor levels are used in the analysis. Two factor levels is the most common number of factor settings in DoE designs because you only need two points to fit a line in a linear regression. However, a larger number of factor levels may be used depending on the type of DoE design. If n factors have two different level settings there will be 2^n total possible combinations of experiments. Table I shows an example of a full factorial experiment with the three designable variables (X_1, X_2, X_3) each run at two level settings. The values of the variable levels are coded so that the high and low level experimental settings are denoted by $+1$ and -1, respectively. The coding normalizes all of the parameters to unitless values which has some beneficial statistical properties [8]. Fig. 1 shows the geometric representation of the experimental design in Table I. The nominal point of the factors, corresponding to zero for the coded factor level settings, is in the center and is surrounded by the experimental level settings at each of the cube's corners. Hopefully, the empirical response model will allow interpolation inside, and perhaps extrapolate a bit outside,

TABLE I
THREE FACTOR, TWO LEVEL FULL FACTORIAL DESIGN

Experiment Number	Factor X_1 Level	Factor X_2 Level	Factor X_3 Level
1	-1	-1	-1
2	-1	-1	+1
3	-1	+1	-1
4	-1	+1	+1
5	+1	-1	-1
6	+1	-1	+1
7	+1	+1	-1
8	+1	+1	+1

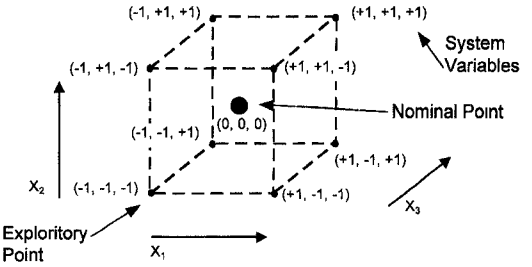

Fig. 1. Geometric representation of Table I experimental design.

the exploration region defined by the cube in Fig. 1 for the example in Table I. Normally, high and low level settings for each factor are chosen with the parameter values that need to be interpolated in-between after the creation of the response model. Therefore, it is extremely important for nonlinear responses that the experimental high and low values are not too far apart as to prevent accurate interpolation of the user defined model. Experiments with more than three factors are difficult to visualize geometrically but follow the same concept presented in Fig. 1.

In the Table I example, the empirical model is built by setting the three factors to the appropriate levels for each experiment and recording the responses for statistical analysis. Regression techniques are then used to fit the recorded response values to a user-defined linear model such as the one shown in (1)

$$y = \beta_0 + \sum_{i=1}^{n} \beta_i x_i + \sum_{i=1}^{n} \sum_{j=1}^{n} \beta_{ij} x_i x_j + \varepsilon_{ij} \quad i \neq j \qquad (1)$$

where n is total number of designable factors, β's are the regression coefficients, and ε_{ij} represents the total error in the regression model. The first term, β_0, in the model is the regression equation's intercept. The second term represents the main factor response effect of the ith factor. The third term in (1) is the joint effect caused by the first order interaction of the i by j main factors. The benefit to this type of simple model is that it easily shows the larger response trends. Simple linear equations do not have any local minima that cause problems for gradient optimizers when finding the best parameter settings. The limitation of this type of modeling is there may be some difficulty using these equations for noncontinuous or quickly changing responses.

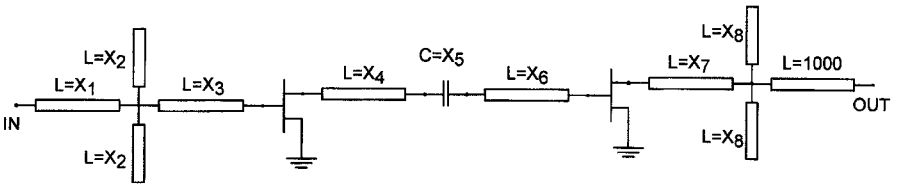

Fig. 2. Two-stage low noise amplifier topology.

Other types of models are available but the most popular for RSM is the quadratic [9], [10]. The quadratic model is the same as (1) except that the $i \neq j$ restriction is removed which requires the factors to have more than just two levels settings. Unfortunately, large number of factor levels dramatically increase the total number of experiments needed to fit the model. Certain DoE's have been designed such as the central-composite and box-Behnken which work well with the quadratic model [7]. The designer must keep in mind that the regression fit is only a simple mathematical model and may not have much physical significance. The model should only be used in the small "exploration region" of parameter space that the DoE was performed. The entire equation would probably change significantly, particularly the interaction terms, when the DoE was performed in another area of parameter space. However, if the empirical model is good then it should enable a designer to optimize their process or circuit within the exploration region even though the model may not hold much physical significance.

As the number of factors increase, full-factorial experimental designs create prohibitively large experimental runs. It would not be unusual to have 10 factors in a DoE which would need $2^{10} = 1024$ total experiments. This many virtual experiments can take a large amount of processing time even with a powerful computer. Furthermore, by using an n-factor full-factorial experiment one obtains information about all possible factor interactions up to and including the interaction term containing all n-factors. Typically, statisticians do not include higher than first order interaction terms, $x_i \cdot x_j$, because the effects due to higher order interactions are difficult to interpret. Therefore, one can reduce the total number of experiments by sacrificing some of the information about the higher order interactions which would have typically been dropped from the empirical model anyway. The type of experimental designs that do not run all of the possible combinations of level settings are called "fractional factorial" designs. These types of designs exhibit *confounding* which means that two or more factor effects can not be separated due to the lack of information. The factors which are confounded can be selected by the user if the experiments are carefully designed. As mentioned before, the second and higher order interactions are usually intentionally confounded so as to obtain a smaller number of experimental runs. Therefore, knowing what effects are confounded is very important. A person can determine which interactions are confounded by examining the *resolution* of the experimental design. "Resolution V" experiments are needed for all model factors in the quadratic form of (1) to be unconfounded with each other. This is the type of resolution that is recommended for response characterization in RSM. Both central-composite and box-Behnken experimental designs are Resolution V [10].

TABLE II
LOW-NOISE AMPLIFIER NOMINAL DESIGN VALUES AND CODING

Variable	Nominal Value	15% (High, +1)	-15% (Low, -1)
X_1	973 μm	1119.0 μm	827.1 μm
X_2	2139 μm	1818.2 μm	2459.9 μm
X_3	4890 μm	5623.5 μm	4156.5 μm
X_4	6879 μm	5847.2 μm	7910.8 μm
X_5	0.9609 pF	1.105 pF	0.817 pF
X_6	6498 μm	7472.7 μm	5523.3 μm
X_7	6099 μm	7013.89 μm	5184.2 μm
X_8	1391 μm	1599.7 μm	1182.4 μm

III. DoE APPLICATION—A DESIGN EXAMPLE

The previous concepts can be applied to statistical modeling of microwave circuits. An example of the methodology has been developed for the two-stage low-noise microwave amplifier shown in Fig. 2. The amplifier was designed to operate in the 4.5 to 5.0 GHz frequency band with over 23 dB of gain and a noise figure less than 1 dB. The input and output match performance goals were both to have a return loss less than -8 dB. The two FET's used in the circuit were arbitrarily picked to be the NEC4583 from an S-parameter database.

Fig. 2 shows the low-noise amplifier had eight designable parameters, variables X_1 through X_8, that were used to adjust the performance of the amplifier. All of the factors were 50 Ω transmission lines lengths except for X_5 which was the value of the DC blocking capacitor. Touchstone was used to optimize the design parameters with the user-defined design goals. The optimized parameter values just met the design specifications and were accepted as being a valid design. These optimized values are listed in Table II and were coded so that they were the nominal (zero) values in a DoE analysis. Table III shows the performance of the amplifier using the Touchstone optimized "nominal values." To achieve a better performance, a SCAD DoE methodology was implemented on the circuit to quantify the design trade-offs and design the better performing circuits listed below the "nominal values" case in Table III. The other cases will be discussed later. The SCAD methodology depicted by the flow chart in Fig. 3 was applied to nominal value circuit design. All of the eight designable variables listed in Table II were identified as the designable factors in a DoE plan.

A full factorial experimental plan, like the one shown in Table I, would require $2^8 = 256$ "virtual" experiments runs. A full-factorial design was impractical both because only the first order interactions were desired in the response model and this designed experiment was being performed by hand. Therefore, higher interaction confounding was intentionally introduced by running a Resolution V DoE which consisted of $2^{8-2} =$

TABLE III
LOW-NOISE AMPLIFIER PERFORMANCE CASES *NOMINAL VALUES OPTIMIZED BY TOUCHSTONE

Response Case	Coded Values								Gain	NF	S_{11}	S_{22}
	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	(dB)	(dB)	(dB)	(dB)
Nominal Values*	0	0	0	0	0	0	0	0	22.96	1.02	-8.11	-10.50
Minimize Noise Figure	0	0	0.2	1	0	1	-0.4	-1	24.92	0.65	-3.94	-6.24
Maximize Gain	0	0	0	-1	-1	-1	-0.3	1	25.05	1.32	-17.94	-19.81
Met All Specifications	0	0	-0.1	0	-1	0	-0.2	-0.1	23.29	0.92	-8.25	-10.35
Good LN Amp	0	1.5	0.1	-0.5	-1	0.5	-0.3	-1.4	23.27	0.80	-11.44	-8.58

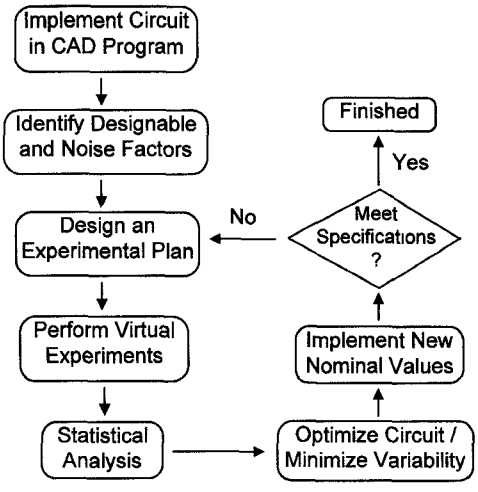

Fig. 3. SCAD methodology for circuit design.

TABLE IV
LOW-NOISE AMPLIFIER MODELED RESPONSE VALUES

Response	R^2
Gain	0.886
Noise Figure	0.803
S_{11}	0.695
S_{22}	0.684

64 experimental runs. Modeling of the quadratic response model was desired so center points were added to make the design central composite fractional factorial. The center points were chosen using the commercial statistical software package SAS® interactive DoE designer which suggested a total of 81 experimental runs [7]. Table II shows the DoE used high and low values that were $\pm 15\%$ of the nominal values which were coded $+1$ and -1, respectively. The responses of interest for each virtual experimental run were the gain, noise factor, S_{11}, and S_{22} of the amplifier from 4.4 to 5.1 GHz at 0.125 GHz steps. These values were recorded in a database for statistical analysis.

SAS® was used to fit the quadratic form of the (1) model for each of the responses at the 4.75 GHz mid-frequency point [9]. The code used to perform the analysis is included in Appendix A. A statistical measure of the regression model's "goodness-of-fit" is called the *R-Square* (R^2) value. In this application, R^2 is the proportion of observed variability in the simulated response that is explained by the regression model. This value is calculated from the total amount of error in the model as identified by (1) and is between the values of zero and one with one indicating the statistical model fits the data with no errors [11]. Table IV lists each response's R^2 value and shows that all of the responses are being modeled reasonably well at the experimental design points. The R^2 is an indication of "goodness-of-fit" only at the actual factor level settings of the experimental runs. The optimal parameter settings for the factors are most likely not to lie at the high, low, or zero factor level settings. Therefore, one is interested in the accuracy of the statistical models in-between our high $(+1)$ and low (-1) level settings. To do this, 20 sets of random parameter values were picked within the limits of each of the experimental factors and the circuit responses for each set were recorded for both the CAD and the statistical model results. The difference between these two values was used to determine the amount of error in the statistical model for the random parameter sets in what could be termed a "reality check." Fig. 4 shows the experimental error for all four responses when the 20 random parameter value sets were used. It can be seen that the models with the largest errors, the input (S_{11}) and output (S_{22}) matches, also had the lowest R^2 values shown in Table IV. However, Fig. 4 shows that "reasonable" results can be achieved through the rather simple quadratic models used for the responses. If the error bounds had been unacceptable then this would have indicated that the DoE was performed with low and high levels that were set too far away from the nominal values. The CAD experiments would then need to be repeated with less variations in the factor level settings. However, in this demonstration one is looking for a trend analysis and very accurate predictive models are not needed.

Once the empirical model is fit using the regression techniques, one can determine which factors, or combination of factors, explain very little of the variation seen in the response data. Those factor terms can be dropped from the model for simplification purposes without sacrificing any significant modeling accuracy. A statistical significance test is performed on each term to determine which can be dropped. In our example, the significance test of each model term was performed using a standard two-tailed t-test at an $\alpha = 0.05$ error level of significance [12]. If the experimental design is orthogonal, then dropping the nonsignificant factor does not change the coefficient values of the other significant factors.

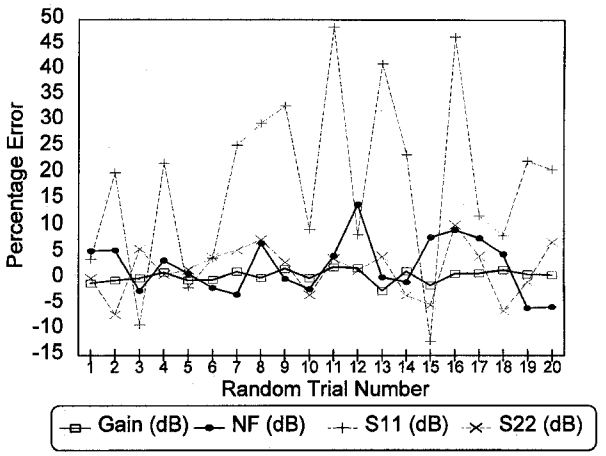

Fig. 4. Model error from random factor settings.

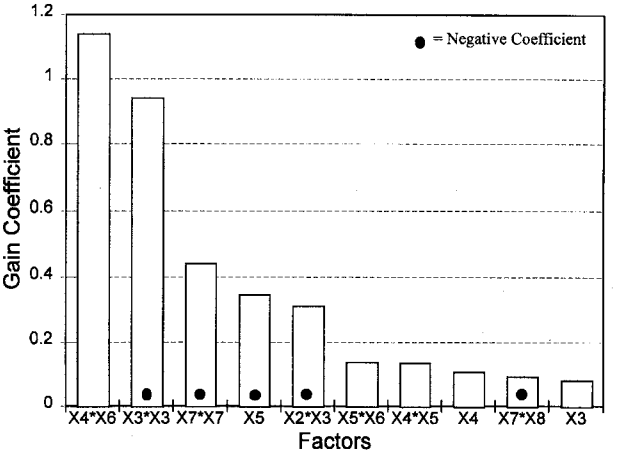

Fig. 5. Pareto of two-stage amplifier gain.

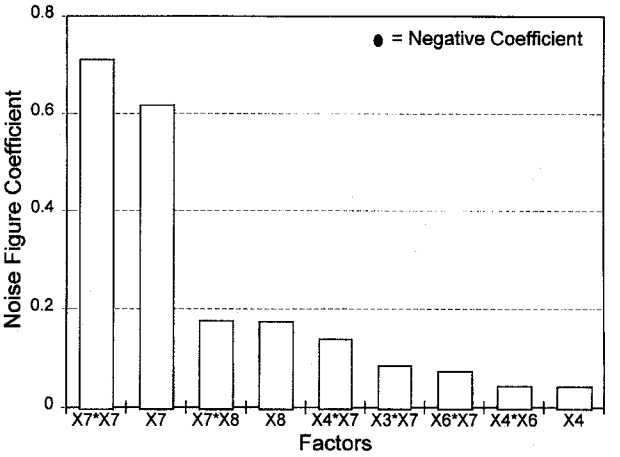

Fig. 6. Pareto of two-stage amplifier noise figure.

However, the quadratic model causes the experimental design to be nonorthogonal and the model's significant terms have to be refit after the nonsignificant factors are dropped. This was the case for the responses in this particular DoE and the regression coefficients were re-estimated with the reduced model. An example of the equation for S_{11} containing only significant factors and interactions is shown below in (2)

$$S_{11} = -7.92 + 2.75X_3 \cdot X_3 + 2.64X_4 \cdot X_4 + 1.72X_6 + 1.04X_4 + 0.62X_2 \cdot X_3 - 0.45X_3. \quad (2)$$

Equation (2) originally had 45 terms, including the intercept, before the nonsignificant factors were dropped leaving only 7 terms in the regression equation. Of course, the number of significant terms varies with the actual response characteristics and number of experimental runs but these examples show that only a few significant factors need to be included in the response model. Deleting nonsignificant terms is usually only done to facilitate writing the equations or to present a reasonable amount of information to the designer.

The most significant factor coefficients in the model for each of the gain, noise figure, input and output match responses were ranked from largest magnitude to smallest and displayed on the Pareto Charts in Figs. 5–7 and 8, respectively. A Pareto Chart is a graphical ranking of the importance of response model effects. Typically, only the statistically significant effects are presented in the Pareto Chart which allow the designer to easily see what influences the response in question. Pareto Charts are commonly used by statisticians and industrial engineers. Referring to (2), one can see each of the significant factor coefficients for the amplifier's input match S_{11} are shown in the Pareto Chart in Fig. 7. Negative coefficients are shown with a dot in the factor's graph bar. The Pareto Charts visually present the circuit's design trade-offs by showing the relative magnitudes of the most significant factors. Ranking the model coefficients from largest to smallest lets the designer see which factors, or combination of factors, account for the most variation in that response. For example, Fig. 5 shows that the interaction between the two transmission line lengths in the matching interstage $(X_4 \cdot X_6)$ has the greatest affect on the amplifier gain. One can also see that the input matching network's transmission line length X_3 has the smallest significant effect on the amplifier gain. It can easily be seen from the Pareto charts that the transmission line length X_1 does not significantly influence any of the responses as would be expected. Therefore, X_1 can be totally ignored in the subsequent analysis and optimization within this volume of design space.

The Fig. 5 Pareto Chart lets the designer visualize that if both the Factor X_4 and X_6 line lengths were increased to the $+1$ and $+1$ factor level settings, then gain of the entire amplifier will also increase because the $X_4 \cdot X_6$ coefficient is positive. If one of the factors was increased while the other was decreased (that is, one at $+1$ the other at -1 causing $X_4 \cdot X_6$ to be -1) then the amplifier gain would tend to decrease due to the positive interaction coefficient. Comparing each of the Pareto charts to each other leads directly to trade-off conclusions. For example, X_4 is shown to be the only main effect factor that affects all the responses significantly. Referring to Fig. 6, decreasing the noise figure (desirable) of circuit in Fig. 2 by making the X_4 factor lower will also decrease gain (undesirable), S_{11} and S_{22} (desirable). The designer can optimize the amplifier by hand choosing the designable parameter values which give the most desirable trade-offs. Once the designer changes the designable

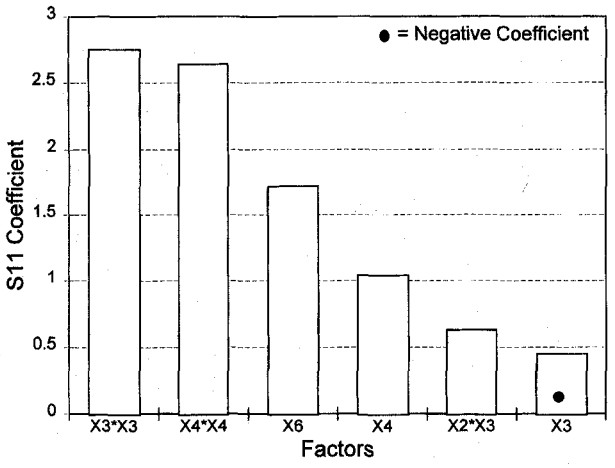

Fig. 7. Pareto of two-stage amplifier S_{11}.

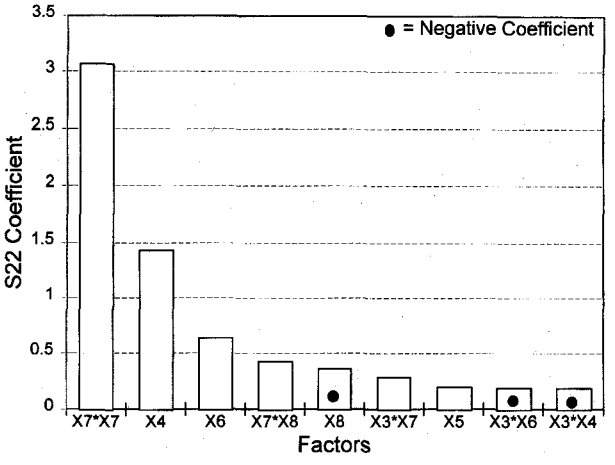

Fig. 8. Pareto of two-stage amplifier S_{22}.

parameters, the design can be resimulated and the performance evaluated. Often, this process would have to be iterated until the design meets the response specifications as shown in the Fig. 3 SCAD methodology flowchart.

The amplifier in Fig. 2 was optimized by hand using the Pareto Charts for several different single frequency performance goals to show the versatility of the SCAD methodology. Each of these performance cases are detailed in Table III along with the coded parameter and performance values. The first two optimization cases, "minimize noise figure" and "maximize gain," used only their respective Pareto Chart to optimize their response regardless of the expense of the other circuit responses. The coded values shown in Table III indicate the designer has tremendous flexibility in optimizing the design using the SCAD methodology. Minimizing or maximizing a response is aided by the fact that the designer has an second order equation for a response which can be easily minimized with respect to a particular variable. Fig. 6 shows an example of this for the amplifier's noise figure which is minimized when X_7 is set to -0.4 level because both X_7 and $X_7 \cdot X_7$ factors are significant.

Both "Met All Specifications" and "Good LN Amp" in Table III were optimized by looking at all of the response Pareto charts in order to evaluate the performance trade-offs. Both cases were obtained only through hand tuning with only the Pareto charts supplying the needed "roadmap" to find optimal parameter configurations. "Met Specifications" in Table III used parameter values which were kept within the $\pm 15\%$ bounds (-1 to $+1$) that the DoE had been performed. However, the "Good LN Amp" case shows that values far outside this range, such as X_2 and X_8, may provide useful optimization points because the general response trends may continue even when the regression models lose accuracy [13]. Finding optimum parameter points may be helped by using linear and nonlinear programming techniques for this type of multiple constrained optimization problem [12]. Taguchi advocated a "pick the winner" scheme of optimization by looking for the experimental run that gives most desirable responses [2]. However, it is not probable that one of the planned experiments would happen to set the circuit's designable parameters at their globally optimum values and this method should not be normally used for optimization.

IV. Variability Reduction

Perhaps the most exciting application of the SCAD methodology is for reduction of circuit response variability. All circuits that are produced have some inherent variability in them. Large circuit variation tends to cause high yield losses. Response variability is due to two types of factors: *designable factor variation and environmental noise*. The effect of designable parameter variation is easily seen by the Pareto charts. Fig. 8 shows that low noise amplifier output match is much more sensitive to the X_4 designable parameter than the X_5 factor. Therefore, if the length X_4 was to vary a small percentage while the circuit was being produced, that would effect the S_{22} response more than if the length factor X_5 were to vary that same percentage. One can see it is in the designer's best interest to reduce the fabrication length variations of the X_4 factor more so than the X_5 factor's length variations. A designer can minimize this propagation of production variation to the circuit responses by using the DoE approach to identify, or screen, the most sensitive parameters and focus effort on controlling their variability [14].

The second type of circuit variability is due to environmental, or "noise," variables such as changes in bias voltages, small signal FET parameters, temperature, or aging. CAD packages can simulate the effect of these variables. The variability due to these parameters can then be minimized by choosing designable parameter settings that cause the circuit to be least sensitive to these noise variables. Often, the designer cannot totally minimize the response variability without miscentering the design. Taguchi described a method of achieving this type of robust circuit design through the use of inner and outer array DoE's [6]. The inner array is the designable factor DoE plan such as the one discussed in the previous section and shown in Table I. The outer array is a separate designed experiment using only the noise variables. When replications are made in actual measurements for a system's particular level settings, the response will not be the same due to measurement error and slightly changing

		Outer Noise Array				
Inner Designable Array		-1	-1	+1	+1	Θ_1
Ψ_1	Ψ_2	-1	+1	-1	+1	Θ_2
-1	-1	y_{11}	y_{12}	y_{13}	y_{14}	
-1	+1	y_{21}	y_{22}	y_{23}	y_{24}	
+1	-1	y_{31}	y_{32}	y_{33}	y_{34}	
+1	+1	y_{41}	y_{42}	y_{43}	y_{44}	

Fig. 9. Inner and outer array DoE Ψ_n designable (outer array) factor, θ_n noise (inner array) factor, and responses y_{ij}.

environmental conditions. In CAD virtual experiments, re-running the same level settings always will give the same response. Therefore, circuit variation must be introduced by using the outer array experiment set as replications of each of the designable parameter array's experiments. Fig. 9 shows an example of an experiment with two designable factor array variables (Ψ_i) being replicated with a full factorial array of two noise factors (Θ_j). The replications across each row will force variability of the response variables for each set of designable factor settings (Γ_i). The variability can be modeled and then minimized by using the designable parameter factors.

Any number of noise factors can be used in the outer array. It should be mentioned that the outer array design can be a fractional factorial because the noise variables are not used as a predictor in the regression model equations. However, large numbers of noise factors can create prohibitively large outer arrays even when highly fractionated factorial designs are used. In these cases, using random permutations to obtain the noise array is suggested. This is equivalent to using the Monte Carlo method to induce variations due to random noise factors in the design. This approach models the true environmental noise more accurately than the method of selecting the noise factor levels. However, to guarantee that the entire noise parameter space is covered, a large number of Monte Carlo level combinations must be made [15]. A SCAD methodology user can use specific noise level settings in order to run fewer total number of virtual experiment simulations when only a small number of noise parameters are being studied. Either approach should give equivalent comparisons of the response variance.

An example of variance reduction will be performed on the single stage amplifier shown in Fig. 10. A circuit with a small number of designable factors was chosen to keep the number of required simulations low. The environmental noise factor chosen was the amplifier's input impedance termination. The amplifier's gain will be affected as the terminating input impedance is changed from the 50 Ω source impedance that was used during the nominal design. It would be desirable to make the amplifier performance insensitive to these variations in the source impedance. DoE provides an easy way to characterize and then minimize this sensitivity. The single-stage amplifier was designed using the microwave CAD simulator Touchstone® with lumped inductors to achieve 50 Ω terminations on both the input and output ports. Afterward, a Taguchi inner noise array was constructed using the four inductor values in a Resolution V Box-Behnken DoE. Table V shows the inductance values and their high and low

TABLE V
SINGLE STAGE AMPLIFIER NOMINAL DESIGN VALUES AND CODING

Variable	Nominal Value	8% (High, +1)	-8% (Low, -1)
L1	5.48 nH	5.92 nH	5.04 nH
L2	11.46 nH	12.38 nH	10.54 nH
L3	14.94 nH	16.14 nH	13.75 nH
L4	0.22 nH	0.24 nH	0.20 nH

TABLE VI
INPUT MATCH TERMINATING IMPEDANCES FOR TAGUCHI OUTER ARRAY

Resistance (Coding)	Reactance (Coding)	Mag(Γ)	Ang(Γ)
50 (Nominal,0)	0 (Nominal,0)	0	0
25 (Low,-1)	-25 (Low,-1)	0.447	-111.7°
25 (Low,-1)	25 (High,+1)	0.447	111.7°
75 (High,+1)	-25 (Low,-1)	0.277	-33.7°
75 (High,+1)	25 (High,+1)	0.277	33.7°

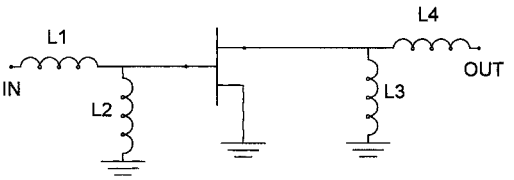

Fig. 10. Single stage amplifier for variance reduction example.

values set at 8% of nominal values in order to get high modeling accuracy. The noise factor array consisted in the termination of the amplifier's input with the five different types of impedances shown in Table VI. Touchstone® defines terminating impedances matches in terms of magnitude and phase of the termination's reflection coefficient, with respect to a characteristic impedance of 50 Ω [16]. The terminating impedances were picked for perfect match and four different quadrants of the Smith chart. The outer noise array consisted of placing each termination on the amplifier's input and calculating the amplifier's gain for each experiment level setting of the inner array.

After the DoE was run, a regression model was used on the gain variance introduced by the different terminations. Equation (3) shows the resulting expression for the gain's variation (dB) with significance of the coefficients determined at an $\alpha = 0.05$ level

$$\begin{aligned}\sigma_{\text{gain}} = {} & 0.96 + 0.328L_1 + 0.081L_2 + 0.232L_3 + 0.024L_4 \\ & - 0.083L_1 \cdot L_1 - 0.062L_1 \cdot L_2 + 0.022L_1 \cdot L_3 \\ & + 0.024L_1 \cdot L_4. \end{aligned} \tag{3}$$

The Pareto Chart of the variance equation's ranked coefficients is shown in Fig. 11 while a Pareto Chart of the amplifier's average gain is in Fig. 12. The regressions models for the gain and gain variance had an R^2 of 0.99 and 0.96, respectively. At the nominal design point (all inductance codings set to zero), the gain was 16.9 dB with a standard deviation of 0.96 dB. Equation (3) and the Pareto chart in Fig. 11 show the total gain variance can be reduced by picking all of the designable parameters at their coded low (-1) values. The amplifier's average gain Pareto Chart in Fig. 12 indicates that picking

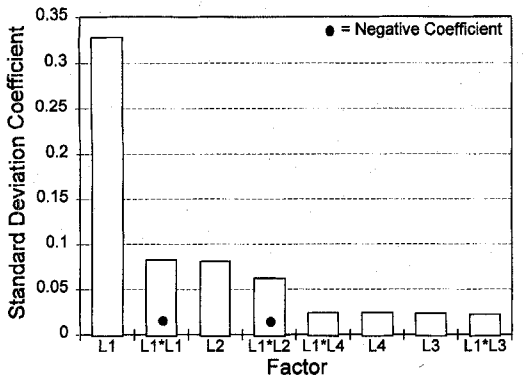

Fig. 11. Single stage amplifier gain variance Pareto Chart accounting for input termination variability.

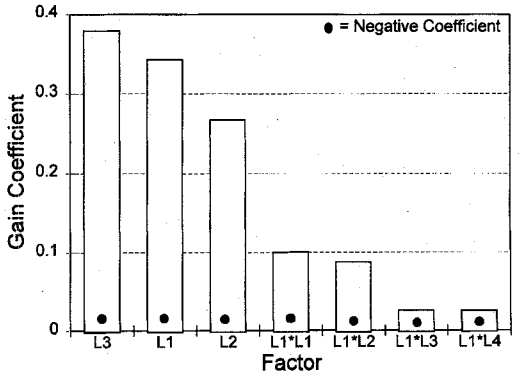

Fig. 12. Single stage amplifier average gain Pareto Chart accounting for input termination variability.

all of the factors at their low (-1) will also tend to increase the gain which is a favorable trade-off. With the new all low designable level settings, the amplifier gain was 17.4 dB, a 0.5 dB increase, while the standard deviation of the gain with respect to the noise variables was reduced 58% to 0.41 dB. This shows that the "by-hand" optimization can both increase nominal value while decreasing the variance of the circuit gain in a straightforward manner.

Another noise factor which affects the amplifier response is active device variations. DoE factors must be orthogonal so the principal component method was chosen to introduce physically realizable FET variations into the DoE noise array [17]. The FET model parameters were varied by changing the first two principal components in the FET model methodology which corresponded to 86% of the total variation in the small signal FET parameters. Picking only some of the principle components enables the outer array to have fewer factors and require a smaller amount of experimental runs. The same inner array DoE as the previous variation model was run for this set of virtual experiments. This resulted in the standard deviation model (in dB) in the following (4) and illustrated in the Pareto Chart shown in Fig. 13 for an $\alpha = 0.05$ level of significance. The R^2 of (4) was 0.99

$$\sigma_{\text{gain}} = 1.283 + 0.489L_1 + 0.162L_2 + 0.022L_4 - 0.063L_1 \cdot L_1 - 0.019L_1 \cdot L_3. \quad (4)$$

The model and Pareto chart indicate that setting all of the

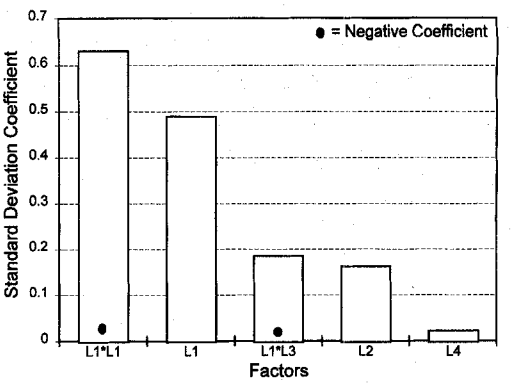

Fig. 13. Single stage amplifier gain variability Pareto Chart accounting for intrinsic FET variability.

factors at their coded low level (-1) will reduce the variations in the circuit's gain response. Coincidentally, these are the same results as were shown when the input termination was used as the noise parameter. Apparently, those settings for the designable parameters create a circuit robust to a variety of environmental factor variations. Also, this example shows that designing a more robust circuit does not always mean sacrificing performance. The principal factor outer array could have been combined with the input termination array, and others, to form one standard deviation model for the amplifier gain but this was not done for example clarity.

V. Discussion of Results

It can be seen that the SCAD modeling methodology gives a reasonably straightforward and systematic way to optimize circuits. There is an effort to integrate these tools directly into the microwave CAD packages so the experimental design, response modeling, and Pareto charts do not have to be done by hand [4], [18]. Currently, these tools use a goal oriented approach with Taguchi loss functions which is slightly different from the approach discussed here. This dissertation shows that minimizing variance in microwave circuit responses is a very exciting area of the SCAD methodology. Robust circuits can be produced in a straightforward manner through the use of the new type of variation introduction and quantification. Other types of responses such as gain ripple, efficiency, or third-order intercept could be modeled and optimized using the SCAD modeling methodology. However, these types of circuit responses are more complex than circuit gain or input match. Our own research into yield modeling has shown that yield response surface is too complex to be modeled with the simple linear regression models advocated in the paper. Modeling over frequency also seems to be SCAD modeling issue that needs to be addressed by future research.

DoE response modeling can also be easily combined with more complex statistical models for predictive circuit response models in a particular region of parameter space. This approach is similar to macro-modeling which has been used to model certain circuits which have slow simulation times [19], [20]. Macro-modeling with SCAD could be implemented for circuits requiring harmonic balance simulations or electromagnetic field solvers. The required experimental simulations

could be done overnight when the computer time is not normally used. The statistical macro-models then could be used, within some bounds of the parameter values, to achieve much faster optimization or design tuning of a circuit. This is especially useful to numerical methods requiring meshing because the empirical response equations will give results that can be interpolated in between mesh points.

VI. Conclusion

A new methodology has been demonstrated for microwave circuit design. The approach uses a combination of statistical experimental design and CAD, called SCAD, and enables a designer to statistically characterize circuit response in a very systematic way. Design trade-offs can be quantified with the simple surface response models from the "virtual" experiments performed by the CAD package. Variation minimization of a circuit's response due to noise parameters inherent in circuits can be achieved with this type of methodology which enables a designer to create robust circuits. The SCAD methodology has been demonstrated on two different amplifier designs each with varying types of designable parameters and optimization goals. Different types of designed experiments were used to show the flexibility of the approach. The introduction of two types of variation noise parameters that are well suited for SCAD, circuit terminations and FET principal components, were also discussed. The SCAD methodology will prove to be an invaluable design tool for a designer making better, more robust circuits that exhibit higher yields.

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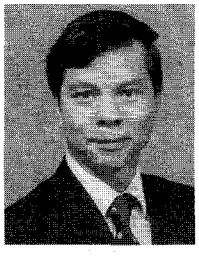

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